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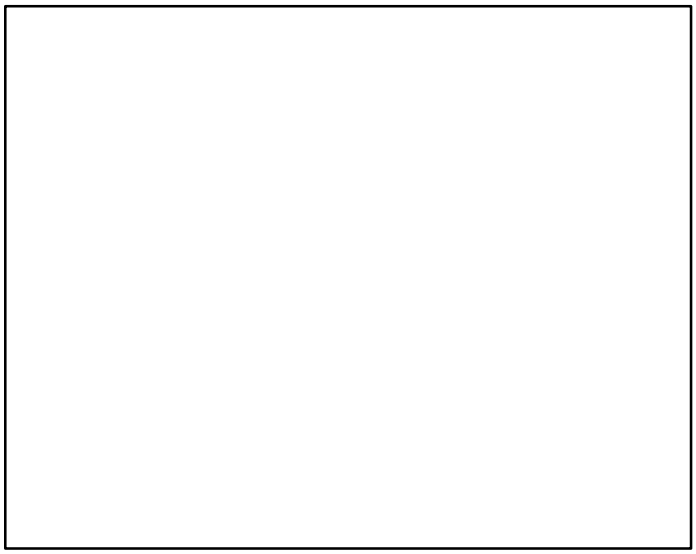


THE "BETTER" PROGRAM

The "BETTER" program is offered on logic only, in dual-in-line ceramic and plastic packages.

Better Processing — Standard Product Plus:

LEVEL II (Suffix D)

- 100% burn-in to MIL-STD-883 test conditions — 160 hours at +125°C or 1.0 eV Arrhenius time/temperature equivalent.
- 100% post burn-in functional and dc parametric tests at 25°C (or max rated T_A at Motorola's option). Maximum PDA of 2% (functional) and 5% (DC and functional).

HOW TO ORDER

MC10101	P	D
Part Identification	Standard Package Suffix	BETTER PROCESSING LEVEL II = SUFFIX D

Part Marking

The Standard Motorola part number with the corresponding "BETTER" suffix can be ordered from your local authorized Motorola distributor or Motorola sales offices. "BETTER" pricing will be quoted as an adder to standard commercial product price.

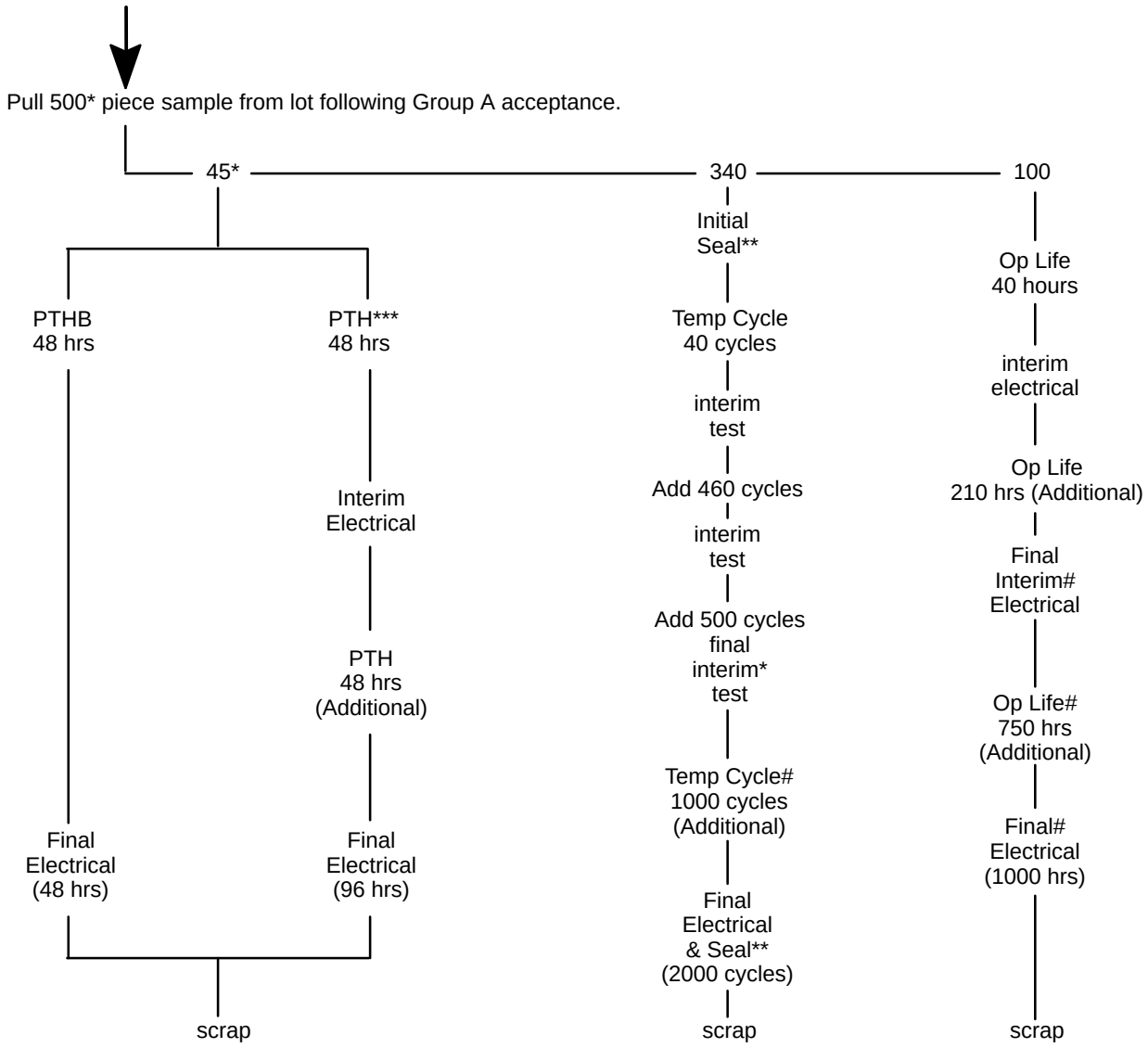
"RAP" Reliability Audit Program for Logic Integrated Circuits

1.0 INTRODUCTION

The Reliability Audit Program developed in March 1977 is the Motorola internal reliability audit which is designed to assess outgoing product performance under accelerated stress conditions. Logic Reliability Engineering has overall responsibility for RAP, including updating its requirements, interpreting its results, administration at offshore locations, and monthly reporting of results. These reports are available at all sales offices. Also available is the "Reliability and Quality Handbook" which contains data for all Motorola Semiconductors (#BR518S).

RAP is a system of environmental and electrical tests performed periodically on randomly selected samples of standard products. Each sample receives the tests specified in section 2.0. Frequency of testing is specified per internal document 12MRM15301A.

2.0 RAP TEST FLOW



One sample per month for FAST, LS, 10H, 10K, MG CMOS, and HSL CMOS.

* PTHB or PTH not required for hermetic products: reduce total sample size to 450 pcs. Additional sample reductions for high pin-count devices per TABLE II notes.

** Seal (Fine & Gross Leak) required for hermetic products.

*** PTH to be used when sockets for PTHB are not available.

3.0 TEST CONDITIONS AND COMMENTS

PTHB — 15 psig/121°C/100% RH at rated V_{CC} or V_{EE} — to be performed on plastic encapsulated devices only.

TEMP CYCLING — MIL-STD-883, Method 1010, Condition C, –65°C/+150°C.

OP LIFE — MIL-STD-883, Method 1005, Condition C (Power plus Reverse Bias), T_A = 145°C.

NOTES:

1. All standard 25°C dc and functional parameters will be measured Go/No/Go at each readout.
2. Any indicated failure is first verified and then submitted to the Product Analysis Lab for detailed analysis.
3. Sampling to include all package types routinely.
4. Device types sampled will be by generic type within each logic I/C product family (MECL, TTL, etc.) and will include all assembly locations (Korea, Philippines, Malaysia, etc.)
5. 16 hrs. PTHB is equivalent to approximately 800 hours of 85°C/85% RH THB for $V_{CC} \leq 15$ V.
6. Only moisture related failures (like corrosion) are criteria for failure on PTHB test.
7. Special device specifications (48A's) for logic products will reference 12MRM15301A as source of generic data for any customer required monthly audit reports.